IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Alfred Wong
Cheng Qian

Serial No. : 10/060,526

Filed : January 30, 2002

For : Delay Reduction of Hardware Implementation of the Maximum a Posterior (MAP) Algorithm

Group Art Unit : 2133

Examiner : Chase, Shelly A.

Atty Docket : / 01-819

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

2/8/05
Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Henry Groth

Reg. No. 39,696

Date: 2/8/2005